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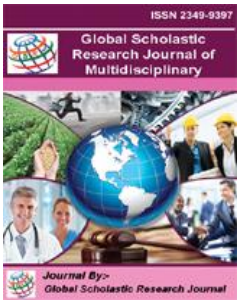

FREQUENCY APPLICATION USING DIGITAL PHASE LOCKED LOOP

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Abstract

The experimental work presented in this paper focuses on the use of digital phase locked loop as a frequency voltage conversion, tone burst generator and frequency synthesizer which is an important application used in the communications and electronics. A Phase locked loop PLL is a frequency selective circuit designed to synchronize with an incoming signal and maintain synchronization in spite of noise or variations in the incoming signal frequency. A digital phase locked loop DPLL integrated circuit IC was employed nominally by MC4046BE.

1. Introduction

A phase Locked loop (PLL) is a system that uses feedback to maintain an output signal in a specific phase relationship with a reference signal, and there's synchronization between its input and output signal. PLL consists of three main components are represented by the block diagram shown in figure 1.

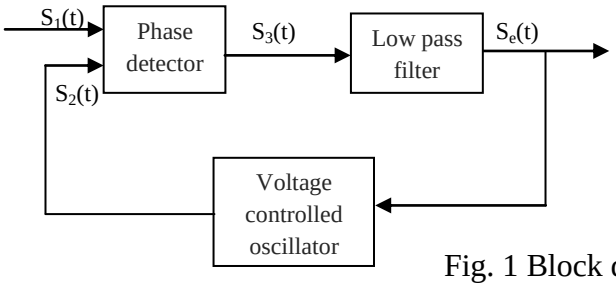


Fig. 1 Block diagram of PLL.

1.1 Digital phase locked loop

The digital phase locked loop (DPLL) has the same construction of the linear phase locked loop except that the DPLL consists of digital and analog components (Hybrid system). The only digital component is the phase comparator and the other components are linear, and contains also an additional block component is a digital counter as shown in figure 2.

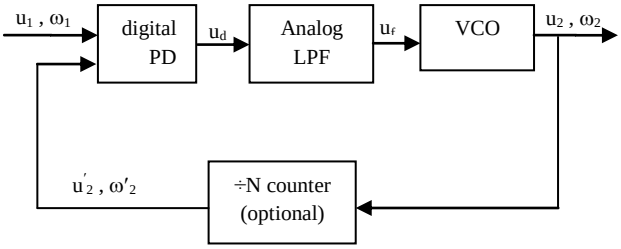


Fig.2 Block diagram of the DPLL.

In the digital phase locked loop, the phase comparator is one of three types: EXOR gate, JK flip-flop and phase frequency detector (PFD). [1][2].

2. PLL characteristics

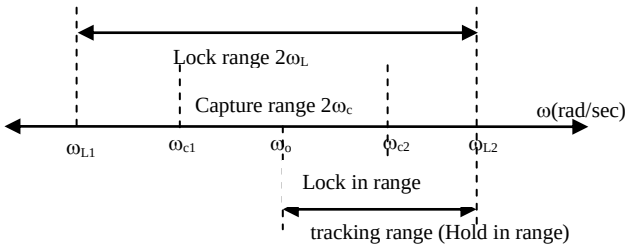
2.1 *Free running frequency (f_o, ω_o)*

Also called the center frequency, this is the frequency which the loop (VCO) operates when not locked to an input signal.

2.2 *The lock range ($2f_L$, $2\omega_L$)*

The range of input frequencies over which the loop will remain in lock. Normally the lock range is centered at the free running frequency. Unless there's some non linearity in the system which limits the frequency deviation on one side of f_o, the deviation from f_o is referred to as tracking range or hold in range as shown in figure 3.

$f_L = 2\ f_H$ ---------- (1) (Hold range)



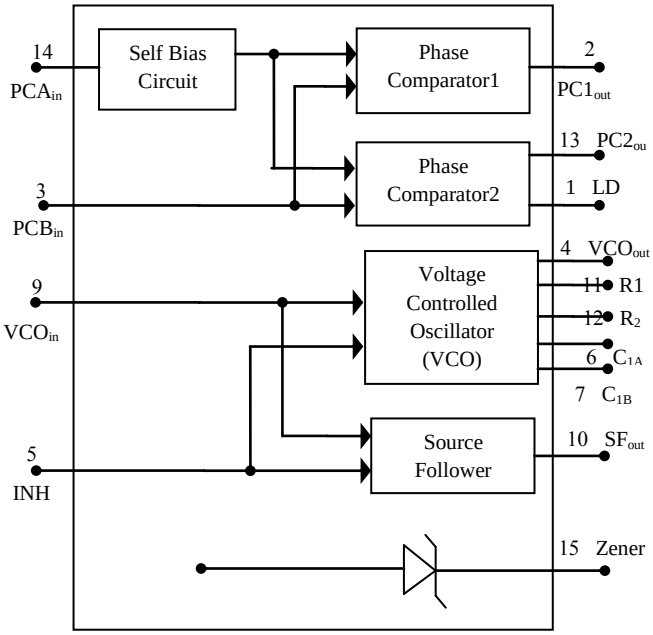


Fig.3 The lock and capture range relationships.

2.3 *Capture range (2fc, 2ωc)*

Sometimes the loop may not be able to acquire lock at the tracking range extremes because of the selectivity afforded by the low pass filter. The capture range is also centered at f_o with equal deviation the capture range is also called the pull-in range . The capture range can never exceed the lock range. [2].

3. Experimental work

The MC4046BE is one of the most versatile CMOS chips, among the many application of the 4046 are those in frequency to voltage conversion, frequency synthesis, frequency modulation, tone decoding, FSK demodulation and frequency multiplication. The 4046 is studied along with its characteristics and applications. Some of these applications have been carried out experimentally. [4].

3.1 *Description of the MC4046BE "DPLL"*

The MC4046BE phase locked loop contains two phase comparators, a voltage controlled oscillator (VCO), source follower and a zener diode. Figure (4-a) is a block diagram of the 4046 CMOS micro power PLL, and figure (4-b) is a pin diagram.

Fig.4(a) Block diagram of MC4046BE.

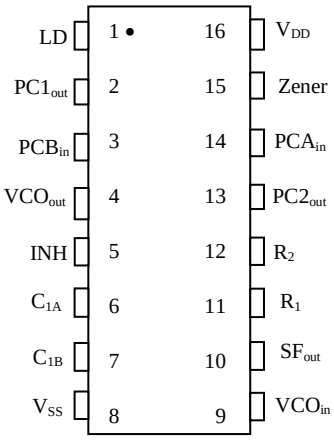


Fig.4 (b) Pinning diagram.

3.1.1 *The phase comparator*

The 4046 includes two phase comparators, they have two common signal inputs PCA_{in} and PCB_{in}. Input PCA_{in} can be used directly coupled to large voltage signals, or indirectly coupled with a series capacitor to small voltage signals.

a) *phase comparator 1*

Phase comparator 1 is an exclusive-OR gate provides a digital error signal PC_1out and maintains 90^o phase shift at the center frequency between PCA_{in} and PCB_{in} signals as shown in figure 5.

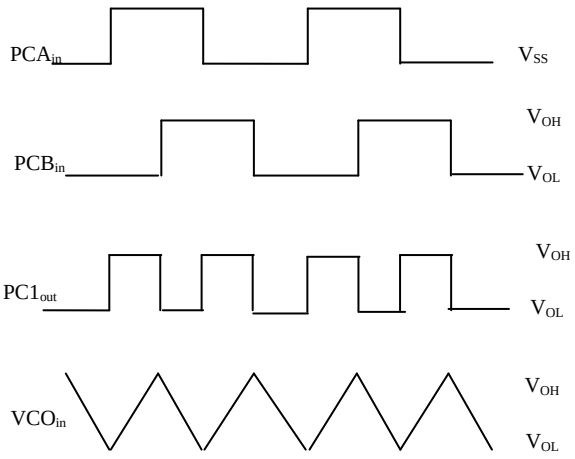


Fig.5 Waveforms of the phase comparator 1.

b) *phase comparator 2*

Phase comparator 2 (with leading edge sensing logic) provides digital error signals and LD, also maintains a 0^o phase shift between PCA_{in} and PCB_{in} signals. The LD output pulse is to determine a PLL is locked or out of lock as shown in figure 6.

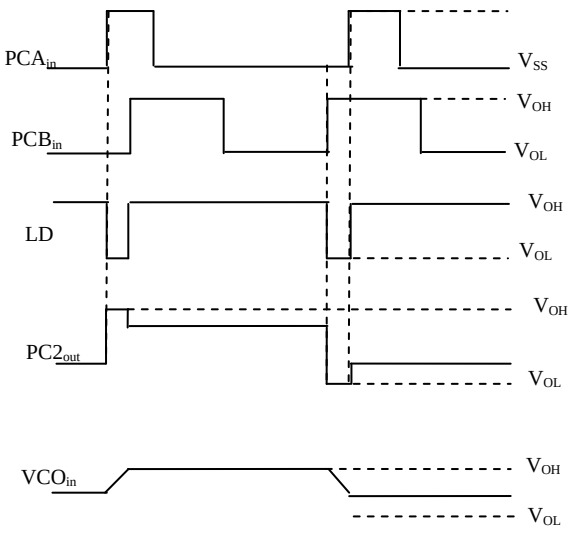


Fig.6 Waveforms of the phase comparator 2.

3.1.2 *Voltage controlled oscillator*

The VCO produces an output signal whose frequency is determined by the input voltage VCO_{in}, the capacitor, and resistors which are connected to pins C_1, R_1 and R_2. These elements are used to determine the minimum and maximum frequency f_{min} and f_{max}.

When only R_1 is used, the VCO frequency can vary from 0 Hz (when the control voltage at pin 9 is V_{ss}) to a maximum frequency. This relation is given by the following equation:

$$f_{max} = \frac{1}{R_1(C_1 + 32pF)} - - - - - (2)$$

When the control voltage is V_{DD}, the minimum frequency will be zero, $f_{min} = 0$, because there's no R_2. When R_2 is included, it's desirable to move the minimum VCO frequency to point above than zero. So R_2 is called the *offset resistor*. This relation is given by:

$$f_{min} = \frac{1}{R_2(C_1 + 32pF)} - - - - - (3)$$

and the other equation:

$$f_{max} = \frac{1}{R_1(C_1 + 32pF)} + f_{min} - - - - - (4)$$

5.1.3 *The source follower*

The source follower output SF_{out} is used with external resistor, where the input voltage of VCO is needed but no loaded can be tolerated. The inhibit input INH (when it's high), disables the VCO and the source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation. The self bias circuit adjusts small voltage signals in the linear region of the amplifier.

3.1.4 *The loop filter*

Employing the MC4046BE any of two external low pass filters may be used. The loop filter looks like the VCO, it also requires a capacitor C_2 and one or two resistors R_3 and R_4 as shown in figure 7.

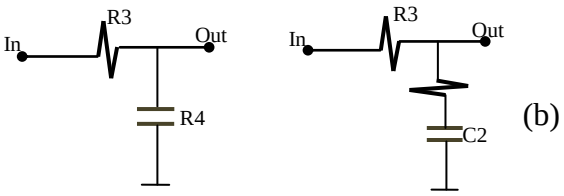


Fig.7 Typical low pass filter used in the MC4046.

The resistance value of R_4 is from 10% to 30% of the value of R_3.

The values of components C_2 , R_3 and R_4 are given by the equation:

$$R_4 C_2 = \frac{6N}{f_{max}} - \frac{N}{2\pi\Delta f} \text{ ------(5)}$$

$$(R_3 + 3000\Omega)\, C_2 = \frac{100 N \Delta f}{f_{max}^2} - R_4 C_2 \text{ -----(6)}$$

where Δf is the frequency deviation is given by:

$\Delta f = f_{max} - f_{min}$ ------- (7)

N is the total deviation ratio in the feedback loop. [2] [3]

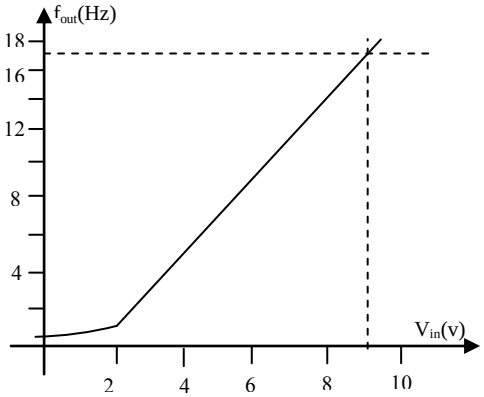
3.2 *Experimental work with MC4046BE "DPLL"*

Some of the important frequency applications are realized practically using the MC4046BE and the experimental results are obtained along with the following experiments.

3.2.1 *Voltage to frequency convertor*

An important feature of the 4046b is that the VCO section can be used on its own for many practical applications. Several of which will be described. Experimenting with them will provide important experience for working with the chip as a complete PLL. Figure 8 shows the most basic 4046 VCO circuit possible for a simple V/f convertor. Varying the input voltage V_{in} from V_{ss} (ground) to V_{DD} will shift the output frequency over a range of 0 Hz (V_{in}= V_{ss} = 0) to a maximum frequency f_{max} at (V_{in}=V_{DD} = 9 V) as given by the equation 2 with V_{DD}=9V, C_1 is selected to be 0.0015μF and R_1=100kΩ with R_2=0. The output frequency versus input voltage values are shown in figure 9 which is almost a linear relationship. Table 1 shows the available values of the input voltage and the output frequency.

Fig.8 A basic 4046 VCO used as V/f convertor.



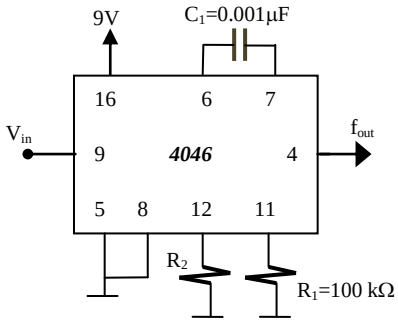


Fig.9 The output frequency versus the input voltage for the V/ f convertor without R_2.

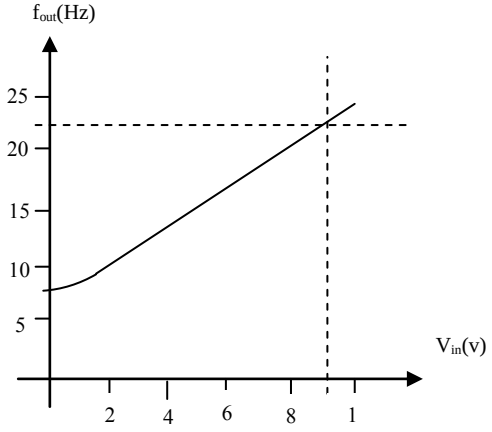
Table 1 The output frequency versus the input voltage.

V_{in}(v)	f_{out}(kHz)
0	0
0.5	0
1.5	0.25
2	1.3
3	3.6
4	6.25
5	8.3
6	10.8
7	12.5
8	14.3
9	16.7

When R_2 is incorporated in the circuit, the output frequency states from f_{min} (rather than 0). It's evaluated from equation 3. Using the same circuit with R_2=220kΩ results the linear relationship between the output frequency and the input voltage as shown in figure 10 and table-2 shows the available values of the input voltage and the output frequency.

Fig.10 The plot of the output frequency versus the input voltage of the V/f convertor with R_2=220kΩ.

Table 2 The output frequency versus the input voltage of the V/f convertor with R_2=220kΩ.



V_{in}(v)	f_{out}(kHz)
0	8.5
1	8.5
2	9.3
3	11.6
4	13.5
5	15
6	18
7	19.2
8	20.8
9	22.7

3.2.2 *Frequency to voltage convertor*

The 4046 can be also used as a micro power frequency to voltage convertor (f/V). Figure 11 shows f/V application circuit. The frequency to voltage convertor may be used as an analog frequency meter to measure the frequency of the input signal. The voltage or current output is directly proportional to the input signal frequency. In figure 11, the input frequency is read out on a 0-1 mA meter connected in series with a 9kΩ load resistor.

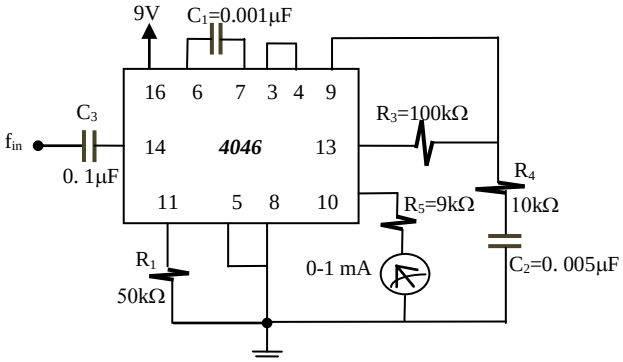


Fig 11 Frequency to voltage convertor as an analog meter.

With the values shown in table 3, the frequency meter has a full scale of 0 to f_{max}. The value of f_{max} is given from the equation 4. The circuit is calibrated by applying 5kHz input signal and adjusting R_1 to produce a meter indication of 0.5mA. The frequency of the input signal is changed and the output current versus the input frequency values are shown in figure 12, which is almost a linear relationship. [1] [6].

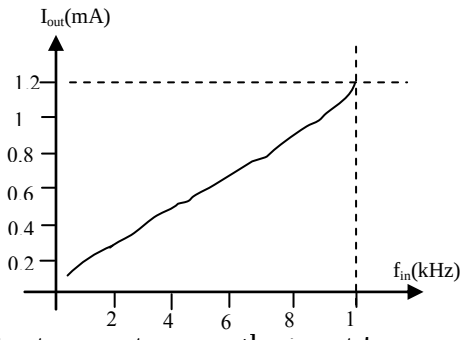


Fig 12 The plot of the output current versus the input frequency of the f/V convertor.

Table 3 The output current values versus the input frequency of the f/V convertor.

f_{in}(kHz)	I_{out}(mA)
0.5	0.07
1.25	0.14
2.27	0.2
3.12	0.31
4.16	0.4
5	0.51
6.25	0.63

7.14	0.75
8.3	0.89
9	1.04
10	1.17

3.2.3 *Tone Burst generator*

Figure 13 shows a simple tone burst generator. An oscillator consisting of two NAND gates (used as an inverter). A 4.7 µF capacitor and a variable resistor R_3 are used to control the oscillator frequency (burst rate). The VCO of MC4046BE is used as V/f convertor and its frequency is varied by the voltage set by the variable resistor R_1. The VCO frequency is maximum when R_1 is in upper position (9V), and minimum when it's in lower position (0V), and thus R_1 controls the tone frequency. When the oscillator output is "high", it disables the VCO, and when it's "low", it enables the VCO output as shown in figure 13. [4] [6].

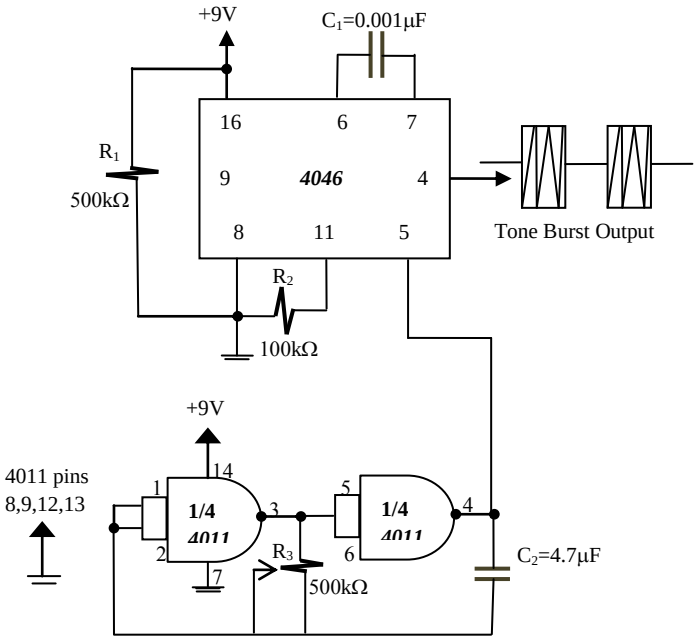


Fig.13 Tone Burst Generator.

3.2.4 *Frequency synthesizer*

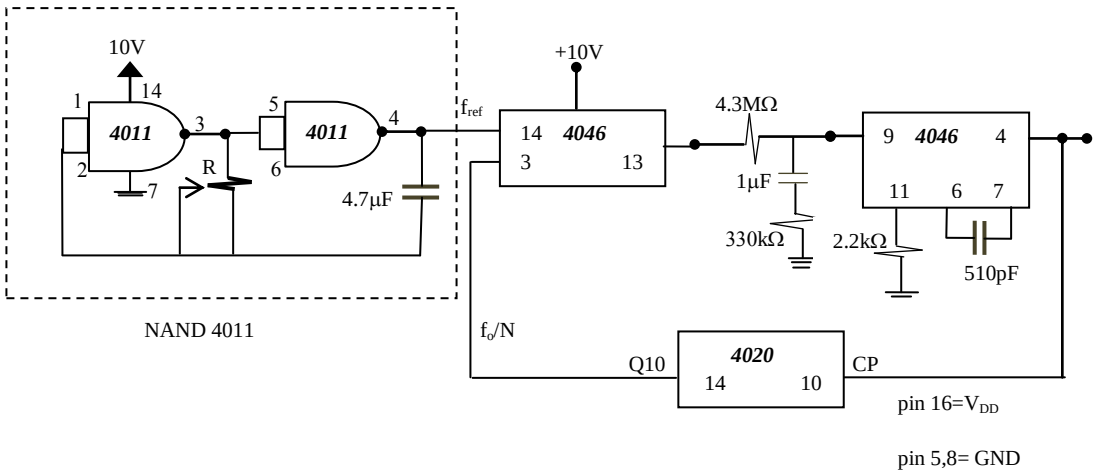
One way to make a practical use of PLL as a frequency synthesizer , a divider is inserted in the feedback loop as shown in figure 14. In this circuit the 4020 counter is counted as a programmable divided by N counter, where N is from 2^0 to 2^{14}. In the operation, the 4011 is two NAND gates oscillator serves as a time based which supply a reference frequency by external elements (4.7 µF and a variable resistor) to the 4046 input. The VCO provides the synthesizer output signal at frequency f_o, the digital programmable counter has an output frequency is determined by the value of N selected by the user. When the loop is locked for a specific value of N then the input frequency is related with the output programmable frequency as given in equation 8.

$f_{ref} = f_o/N$ ---------- (8)

The synthesizer output is:

$f_o = N. f_{ref}$ --------(9)

Fig.14 Frequency synthesizer based on CMOS4046



In this experiment with N=1024, the following frequencies are synthesized as shown in table 4.

Table 4 the output synthesized frequencies in three different values.

f_{ref}(Hz)	91	96	114
f_{syn}(kHz)	100	111	125

For the best applications and precision results, it's used the crystal controlled time base, if the input signal is stable frequency then at locking the output frequency gives multiple stable frequencies from one frequency value. [1] [6].

4. *Conclusion*

- ✓ The phase locked loop operates by producing an oscillator frequency to match the input frequency. In the locked condition any slight change of an input frequency, first appears as a change in phase between input and oscillator frequency, this phase shift then acts as an error signal to change the frequency of the local PLL oscillator and match the input signal frequency.

- ✓ The locking onto a phase relationship between the input frequency and the local oscillator accounts for the name *PHASE LOCKED LOOP*.

- ✓ The PLL is a complete working system that can be used to send and receive signals. In fact the PLL can create, select, decode and reproduce a signal.

- ✓ Selection of free running oscillator frequency and changing it by a control voltage makes the VCO well suiting for converting digital data that is represented by two different voltage levels into different frequencies. A "1" voltage level can be related to a frequency called a mark (normally 2000Hz), and a "0" voltage level to a frequency called a space (normally 1500Hz). This technique called Frequency Shift Keying "FSK" is typical of data being transmitted over telephone and radio links where it's impractical to use DC voltage level shifts.

- ✓ Essentially this is what a modem (modulator demodulator), as it converts data to tones, then it reverses the process and converts the received tones to "1"s and "0"s at the receiver of the system to use.

- ✓ If the input signal frequency variation enters to the phase comparator input, we get an output voltage (corresponding to this frequency) after low pass filter. This is frequency to voltage conversion.

- ✓ When the VCO shifts frequency and locks to the input, the frequency will duplicate, if the input signal contains static noise, the VCO output will be an exact reproduction of the signal frequency without the static noise. Thus the PLL has accomplished signal reconditioning or reconstitution.

- ✓ The VCO is exactly synchronized with an incoming signal, it can be amplified, filtered and used to "Clock" the signal or give synchronizing information necessary to lock at the input signal.

- ✓ If the programmable counter is inserted between the VCO and the phase comparator . at the locking condition we can get the output frequency that is a multiple of the input frequency (frequency synthesis). Using crystal stabilized input frequency, we can get multiple crystal stabilized frequencies from this one stable input frequency.

- ✓ In the experimental work using MC4046 , the calculated frequency values may be in error with the practical values by as much as factor of 4. This poses no problem because it's a simple matter to use trimmer potentiometers for resistors and to adjust them to get the desired frequency range. [1] [2] [4].

5. *References*

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