Evaluation of Modulation Techniques for 5-Level Inverter Based on Multicarrier Level Shift PWM

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***Abstract*—Multilevel inverter has become attractive in the power industries and it can be applied in many applications especially in renewable energy systems and improvement of the power quality. On the other hand, the technique used to generate the required switching pulses plays an important role to improve the inverter characteristics. The paper presents an assessment of three different types of control techniques based on multicarrier level shifted PWM (S-IPD, S-POD and S-APOD) applied to a single phase full bridge five level diode clamped inverter. The main parameters considered are the Total Harmonic Distortion (THD) and harmonic spectrum. The reported results are based on the experimental and simulation realization. In addition, the simulation and experimental output voltages and currents waveforms of all mentioned techniques are presented.**

***Keywords*—Five level DC inverter, level shifted PWM, S-IPD, S-POD and S-APOD.**

I. INTRODUCTION

The growing attraction of high and medium power application in utility, industrial, and renewable energy systems has increased the demand for high and medium power inverters. However, due to the maximum voltage rating of switches, connecting only one power semiconductor switch directly to the high voltage is a problematic. To address this problem, a multilevel power inverter structure has been introduced as an alternative in high and medium voltage situation. The basic concept of power inversion in multilevel inverters is based on a series connection of switching components with several lower DC voltage sources to synthesize staircase voltage waveform. Different sources such as capacitors, batteries or renewable energy can be considered as DC voltage sources in various multilevel inverter structures [1].

The most common multilevel inverter topologies are known as Diode clamped Cascade and flying capacitor. For switching of these topologies, various modulation strategies have been already reported. Among them the Carrier-based and Space Vector Modulation methods are the most popular ones. The method of Multi-level space vector modulation, have been extended from its two-level version, involves switching of the three nearest voltage vectors to the reference one. Several approaches have been already presented to show how these space vectors can be found and selected for the particular operating conditions. However it is likely that carrier-based strategies will remain widely adopted because of their inherent simplicity and reduced computational requirements. For Diode-clamped inverters, carrier-based modulation strategies are commonly established based on the carrier disposition technique, while for cascade inverters; the phase shifted technique is widely used. Modulation strategies have a wide range of features which can be desirable or undesirable for a specified application [2]-[4].

II. FIVE LEVEL POWER CIRCUIT TOPOLOGY

There are three main topologies of multilevel inverter. Cascaded H-bridges, Flying-capacitors and Diode-clamped multilevel inverters. The topology that have been used in this paper is a single phase full bridge five levels diode clamped inverter and this topology is shown in Fig. 1.

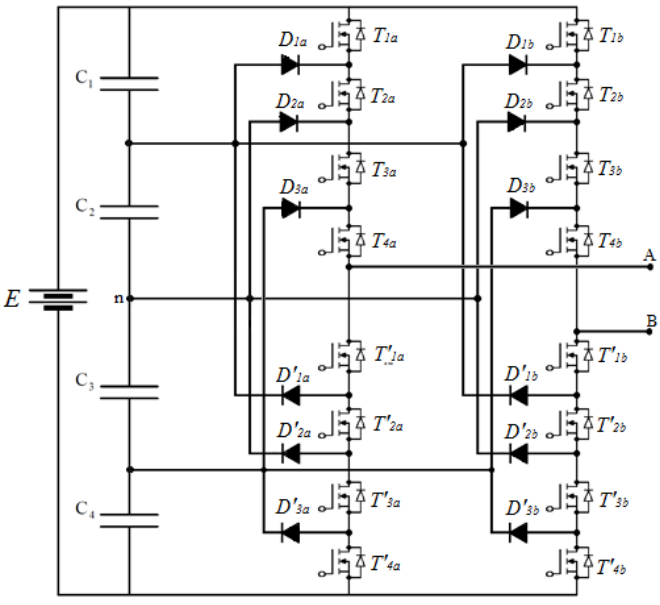


Fig. 1.Single phase full bridge five levels diode clamped inverter.

The m-level diode-clamped inverter leg has ***(m-1)*** dc link capacitors, ***2(m-1)*** switches, ***m-levels*** output phase voltage and ***(2m-1)*** levels output line voltage. Although each active

switching device is required to block only a voltage level equal to the capacitor voltage of $V_c = E / (m-1)$, the clamping diodes require different ratings for reverse voltage blocking. If the inverter is designed such that each blocking diode has the same voltage rating as the active switches so D_{nx} where n is (1 , 2 or 3) and x is(a or b) will require n diodes in series; consequently, the number of diodes required for each phase leg would be $(m-1) \times (m-2)$ and the minimum diode reverse voltage is equal to the capacitor voltage $V_{rmin} = V_c = E/(m-1)$[5]. Also, the switching states of the inverter are summarized as shown in the table I.

TABLE I

5-LEVEL DIODE-CLAMPED LEG RELATIONSHIPS BETWEEN CONFIGURATIONS AND OUTPUT VOLTAGES.

Switches states								
T_{1a}	T_{2a}	T_{3a}	T_{4a}	T'_{1a}	T'_{2a}	T'_{3a}	T'_{4a}	V_{An}
1	1	1	1	0	0	0	0	$E/2$
0	1	1	1	1	0	0	0	$E/4$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-E/4$
0	0	0	0	1	1	1	1	$-E/2$

Making some generalization from Table I. In a *m*-level diode-clamped leg there are no intra-phase redundant states and $(m-1)$ consecutive switches are conducting. Moving the series of conducting switches from the top to the bottom end of the leg, the output voltage decreases from ***E/2 to -E/2*** if the output is taken from V_{An} [5],[6].

III. IMPLEMENTATION OF MODULATION TECHNIQUES

The evaluations of modulation techniques that have been used to control the switches of the inverter are the heart of this topic and there are lots of techniques summarized in Fig. 2, according to [5]. In this paper three modulation techniques have been conducted based on multi carrier level shifted PWM using sinusoidal reference signal and they are considered popular methods in industrial application.

The operation principle of all the three techniques is as follow: for a *m*-level multilevel inverter, $(m-1)$ carriers with the same frequency f_c and the same peak-to-peak amplitude A_c, but translated in levels are disposed such that the bands they occupy are contiguous. There are two reference signals out of phase each has peak-to-peak amplitude A_r and frequency f_r, and they are centered in the middle of the carrier set. The two references are continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on; and

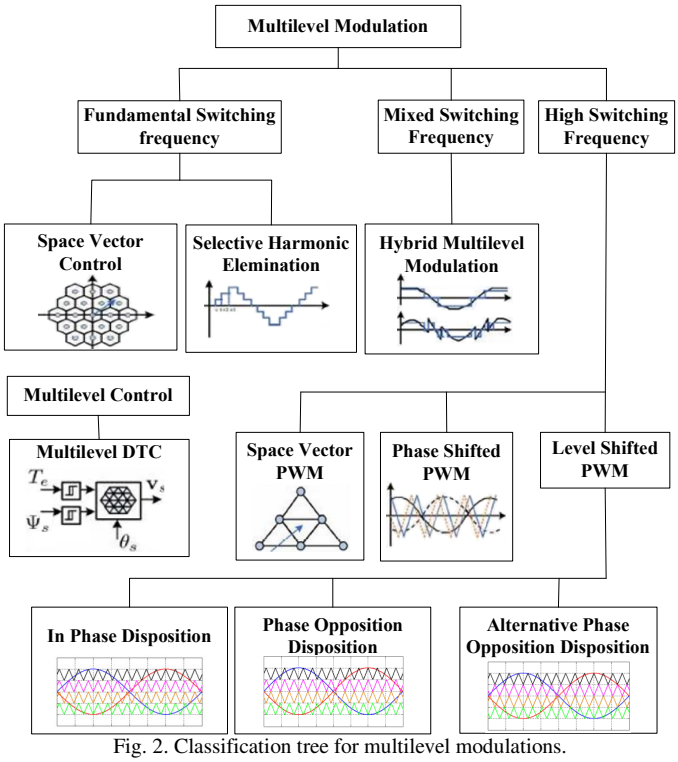


Fig. 2. Classification tree for multilevel modulations.

if the reference is less than a carrier signal, then the active device is switched off as shown in Fig. 3. In multilevel inverters, the amplitude modulation ratio, m_a, and the frequency modulation ratio, m_f are defined as follow [5], [7]-[8]:

$$m_a = \frac{A_r}{(m-1) * A_c} \quad (1)$$

$$m_f = \frac{f_c}{f_r} \quad (2)$$

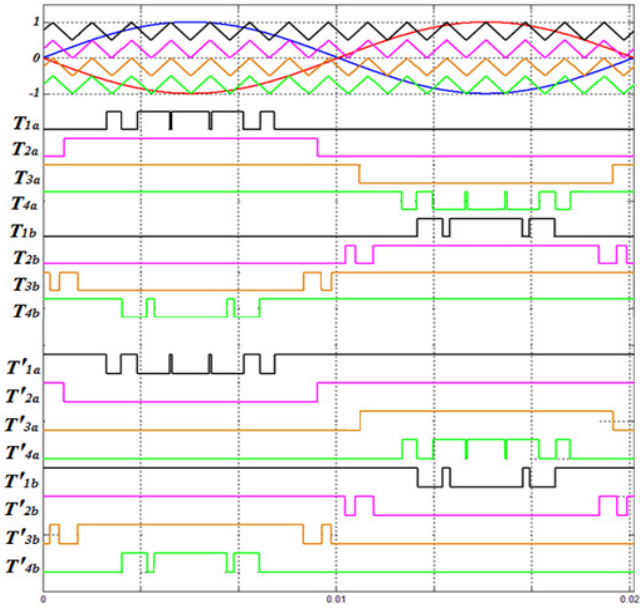


Fig. 3. The level shifted PWM technique with the train of pulses used to control the single phase full bridge five level inverter , $m_a=1$,$m_f= 15$

In this paper three modulation techniques have been studied and they are as follow:

A. *Sinusoidal reference In Phase disposition technique (S-IPD).*

In this method the carriers are the same in the frequency, amplitude and phases, they are just different in DC offset to occupy contiguous bands. The waveforms of the carriers of this technique with sinusoidal reference is illustrated in Fig. 4.

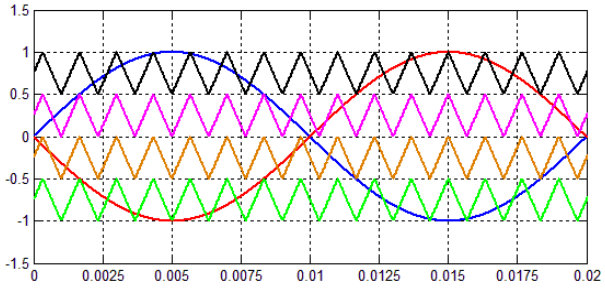


Fig. 4. S-IPD technique, ma=1 ,mf= 15.

B. *Sinusoidal reference Alternative Phase Opposition Disposition (S-APOD).*

In this method the carriers have the same frequency and the same amplitude but they are different in their DC offset and their phases are different where each carrier band is shifted by 180 degrees from the adjacent bands. The waveforms of the carriers of this technique with sinusoidal reference is illustrated in Fig. 5.

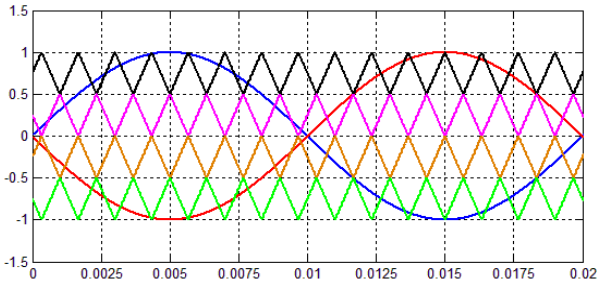


Fig. 5. S-APOD technique , ma=1 ,mf= 15

C. *Sinusoidal reference Phase opposition disposition (S-POD).*

Carriers in this method are the same in frequency and amplitude but they are different in phase and DC Offset where the carriers above the zero reference are in phase but shifted by 180 degrees from those carriers below the zero reference. The waveforms of the carriers of this technique with sinusoidal reference are illustrated in Fig. 6.

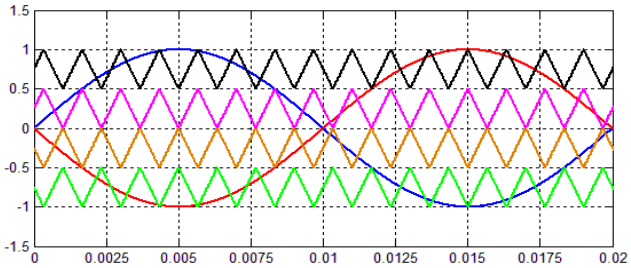


Fig. 6. S-POD technique, ma=1 ,mf= 15

IV. SOFTWARE AND HARDWARE.

It should be noted that this study is conducted on a laboratory setup with the only objective of testing modulation techniques

A. *Software.*

Each technique is realized by means of a computer program that generate the required control signals to the power transistors via the parallel port, the program requires the values of amplitude modulation ration (*modulation index, m_a*) and frequency modulation ratio (m_f) in addition to the type of technique under consideration. Computer programming was used to realize the program according to the flowchart shown in fig. 7.

B. *Hardware*

Once the generated signals are output from the computer's parallel port (8 lines for T_{1a} to T_{4a} and T_{1b} to T_{4b}), the following hardware components are added (refer to fig. 8):

1. Logic Inverters 4704 to obtain the signals for T'_{1a} to T'_{4a} and T'_{1b} to T'_{4b}.
2. Isolation circuit, the goal is to isolate the computer from the power circuit and to prevent short circuit occurrence between switches. For isolation the IC 4N25 (16 units) is used.
3. For the power switches of the main inverter the IRF530 MOSFETs (16 units) have been used.
4. The clamping diode that has been used in the circuit is BY359-1500 diode (12 units).
5. Four DC supply each of V_{dc}=27v to construct the full DC-link voltage.
6. The AC-load that has been used is reactive load of 100mH inductor with rated current of $I_{L\text{-}rated}$=0.5A and 200Ω resistor.

Finally Fig. 9, shows a photo of the overall setup of the experimental single-phase full bridge five level inverter considered in this paper.

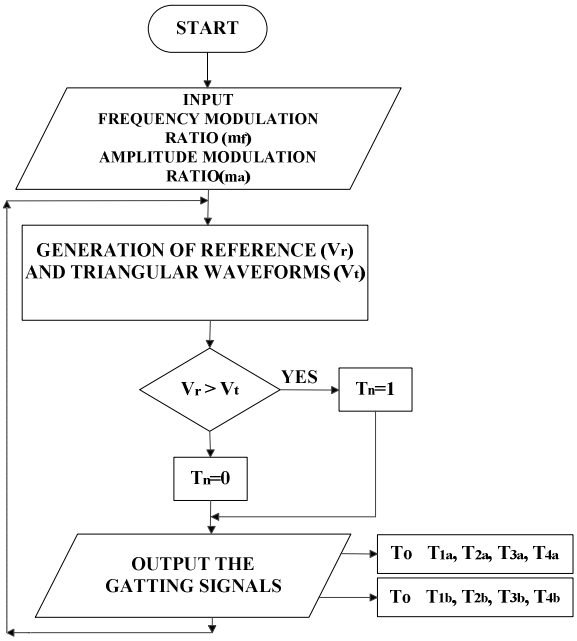


Fig. 7. Algorithm software for gating signals generation.

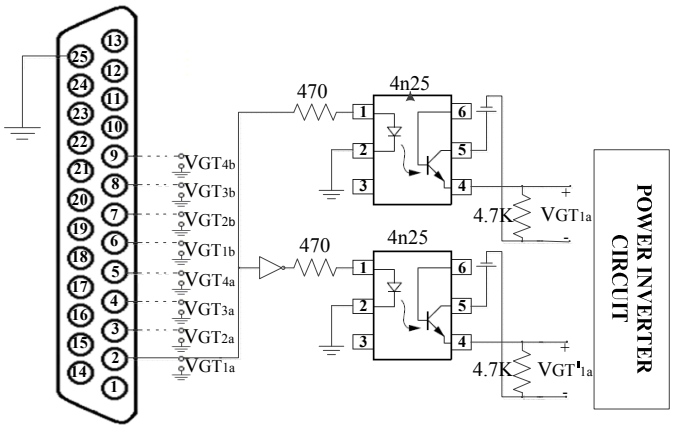


Fig. 8. Hardware block diagram for five level inverter.

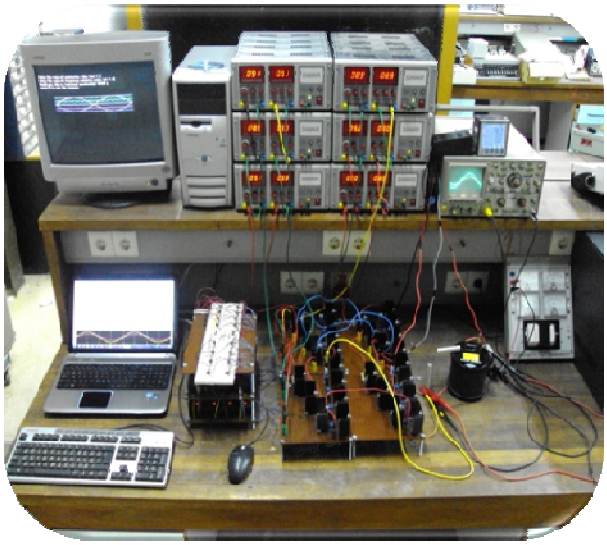


Fig. 9. A photo of the overall setup of the experimental single-phase full bridge five level inverter.

V. SIMULATION AND EXPERIMENTAL RESULTS.

The gating signals necessary for the operation of the single phase full bridge five level inverter using the different three techniques considered in this paper is conducted using the MATLAB Simulink for different cases of operation. In other hand, the hardware shown in Fig. 8, is implemented experimentally in the lab, whose operation is tested for different cases in all the three techniques, some of them are selected for the presentation in this paper. The main criteria for the judgment of the quality of the specified technique is mainly the THD and the harmonic spectrum for different values of m_f (Frequency Modulation Ratio) and m_a (amplitude modulation ratio); in addition the output voltage waveforms are obtained.

Fig. 10, to Fig. 15, present the simulation and experimental results of the output voltage and current waveforms and the harmonic spectrum of the output voltage at m_f =18, m_a =1 to make comparison between all the three techniques.

In order to show the closeness between the simulation and experimental results from the THD point of view Fig. 16, shows the ***THD vs*** $\boldsymbol{m_a}$ at m_f =18 for S-IPD technique via simulation and experimentally.

In order to make the comparison between the three techniques related to the THD, Fig. 17, shows the ***THD vs*** $\boldsymbol{m_a}$ for all the three techniques at m_f =18 experimentally.

Fig. 18, shows the output voltage RMS value versus m_a ($\boldsymbol{V_{rms}}$ ***vs*** $\boldsymbol{m_a}$) for all the three techniques experimentally .

Table II, summarized the values of THD% for multiple values of m_a for m_f =15 and 18 for the three techniques.

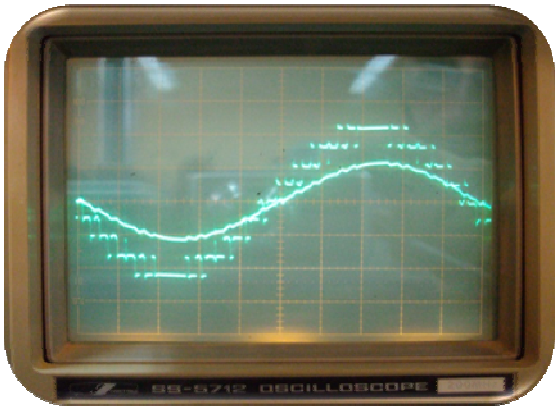
TABLE II
THD – m_a OF THE OUTPUT VOLTAGE FOR THE THREE TECHNIQUES, AT m_f =15 AND 18

Tech.	S-IPD		S-POD		S-APOD	
m_f	15	18	15	18	15	18
m_a	THD%	THD%	THD%	THD%	THD%	THD%
0.3	30.1	29.9	89.3	86.3	89.2	85.7
0.4	25.2	23.8	62.7	60	63.9	60.3
0.5	19.3	18.6	42.2	41.3	41.8	40.7
0.6	16.4	16	34	31.8	33.8	31.7
0.7	14.8	14.6	32.3	30	32.5	30.4
0.8	12	11.8	31.2	29.1	30.5	29.1
0.9	11.7	11	27.1	25.4	27.2	25.3
1	9.5	10.7	20.9	20.8	21.1	21.2
1.1	9	9.5	18.1	17.3	18.2	17.4
1.2	9.7	9.1	17.5	15.7	17.6	16.4
1.3	11.2	11.3	17.7	16.3	17.8	17.2
1.4	13.7	13.8	18	18	18.3	18.1
1.5	16.2	14.7	18.9	18.6	19.6	19.1

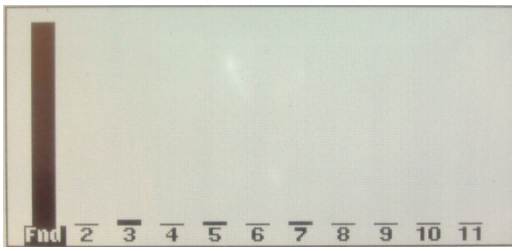
VI. DISCUSSION OF RESULTS.

From the output voltage waveform point of view it is clear that the output voltage waveforms produced from the *S-IPD* technique at m_a=1 and m_f =18 are constructed of 9-levels even though the inverter is a single phase 5-levels. Each level has an amplitude equals to V_{dc}. The output voltage waveforms produced from the other techniques (S-POD and S-APOD) at m_a =1 and m_f =18 are constructed of 5-levels, each level has an amplitude equals to 2Vdc resulting in higher dv/dt stress on the components in comparison to S-IPD. Even-though the inverter that has been implemented in this paper is a single phase full bridge 5-level inverter, the number of level produced by the *S-IPD* technique differ from five levels depending on amplitude modulation ratio (m_a). It produces 9-levels which seems to be a 9-level inverter at $m_a \geq 0.75$, and it produces 7-levels which seems to be 7-level inverter at $0.5<m_a<0.75$, and it produces 5-levels which seems to be 5-level inverter at low amplitude modulation ratio $0.25<m_a<0.5$.

The number of levels produced from the *S-POD and S-APOD,* techniques are 5- levels if $m_a>0.5$, and 3-levels if $m_a \leq 0.5$ (i.e. low amplitude modulation ratio) which means that the multilevel inverter seems to be 3-level inverter and it will not make use of all of its levels.

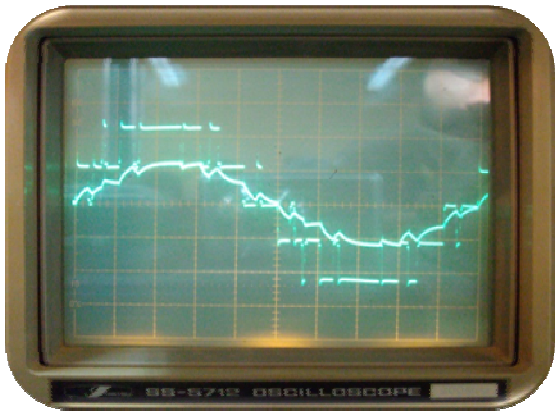


(a)ch1(50v/Div), ch2(0.8A/Div) , 2ms/Div

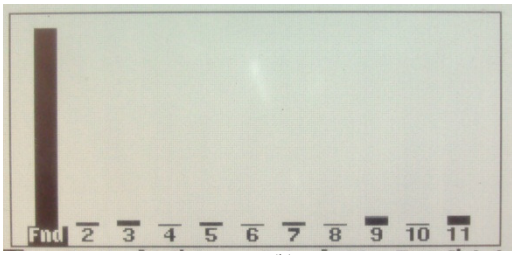


(b)

Fig. 10. S-IPD, ma =1 , mf =18, (a) experimental output voltage and current; (b)output voltage harmonic spectrum

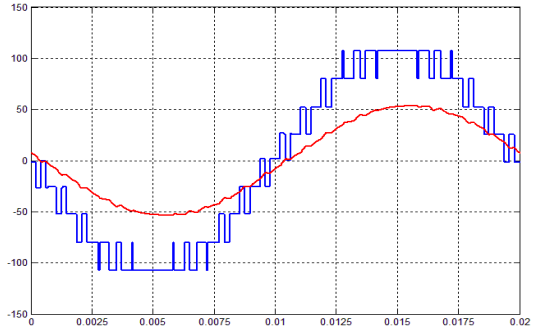


(a)ch1(50v/Div), ch2(0.8A/Div) , 2ms/Div

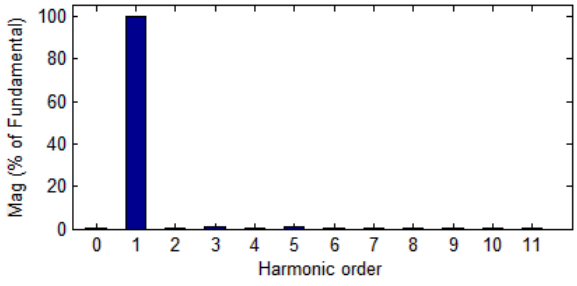


(b)

Fig. 12. S-POD, m_a =1,m_f =18, (a) experimental output voltage and current; (b)output voltage harmonic spectrum

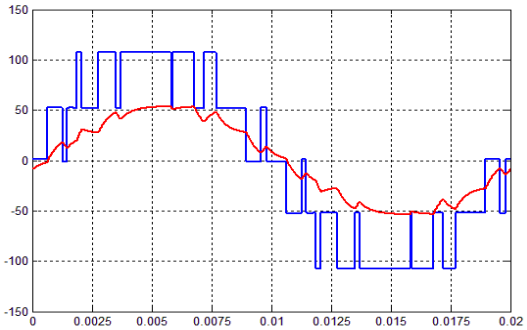


(a)output current enlarged with scale 100

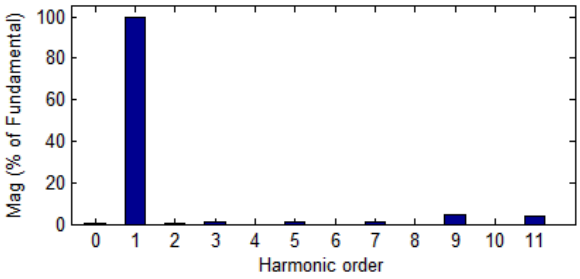


(b)

Fig. 11. S-IPD, m_a =1 , m_f =18, (a) Simulation output voltage and current(b); output voltage harmonic spectrum

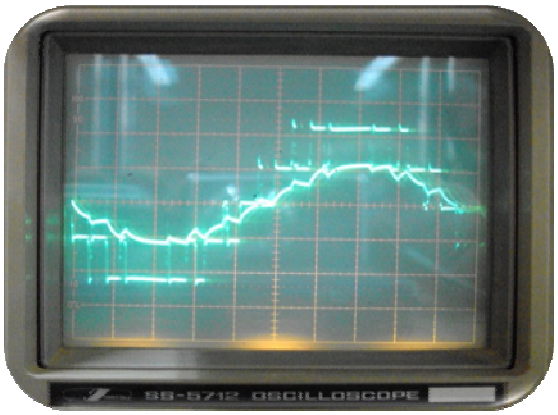


(a)output current enlarged with scale 100



(b)

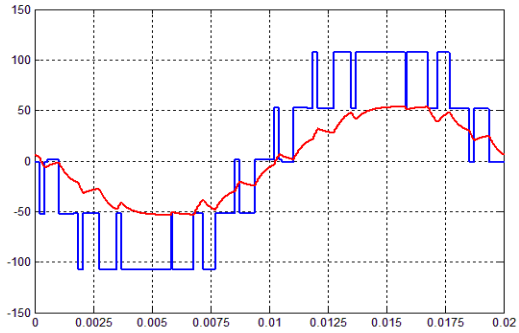
Fig. 13. S-POD, m_a =1 , m_f =18, (a) Simulation output voltage and current; (b)output voltage harmonic spectrum



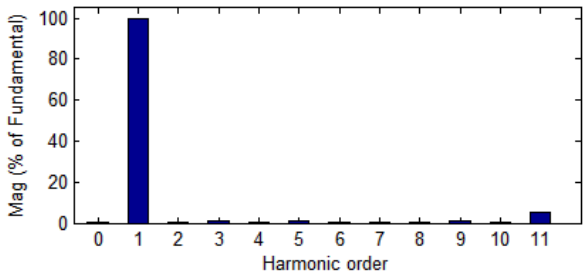
(a)ch1(50v/Div), ch2(0.8A/Div) , 2ms/Div

(b)

Fig. 14. S-APOD, m_a=1,m_f =18,(a) experimental output voltage and current; (b)output voltage harmonic spectrum



(a)output current enlarged with scale 100



(b)

Fig. 15. S-APOD, m_a =1 , m_f =18, (a) Simulation output voltage and current; (b)output voltage harmonic spectrum

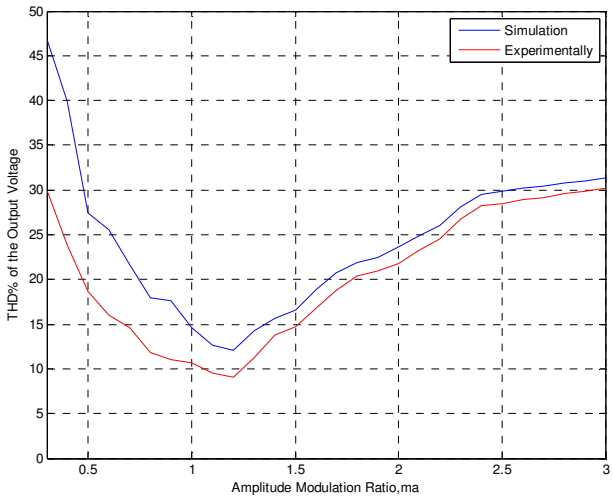


Fig. 16. THD vs m_a of the output voltage at m_f =18 for S-IPD technique via simulation and experimentally.

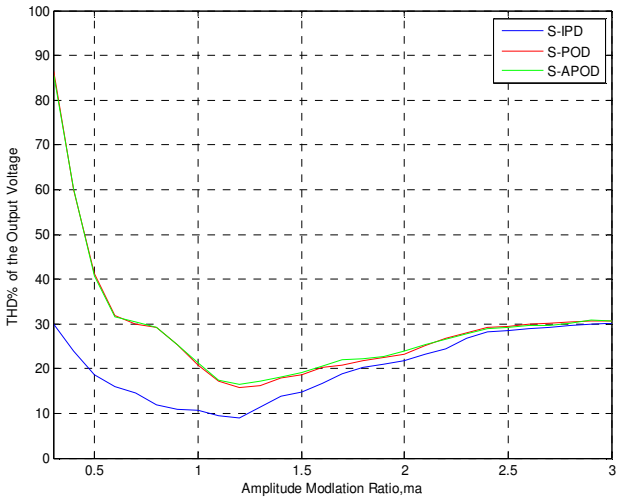


Fig. 17. THD vs m_a at m_f =18 for the three techniques experimentally.

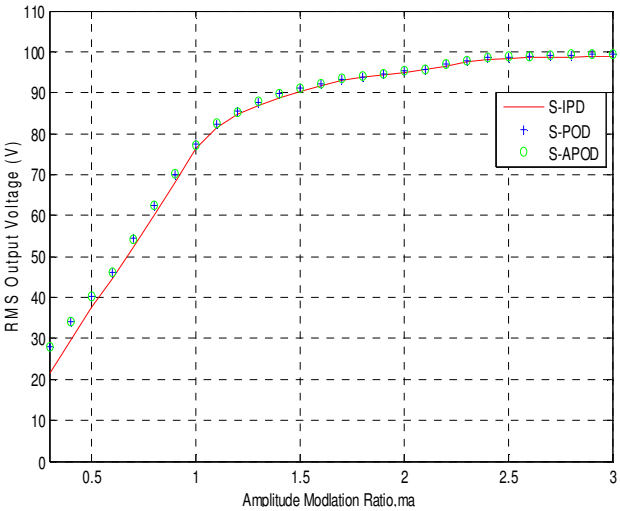


Fig. 18. V_{rms} vs m_a at m_f =18 for the three techniques experimentally.

It is obvious that the technique that gives the higher number of levels is better because it will give lower THD and table III, summarized the number of produced levels for different value of m_a for the all techniques.

TABLE III
THE NUMBER OF PRODUCED LEVELS FOR DIFFERENT VALUES OF m_a

Amplitude Modulation Ratio	Number Of Produced Levels	
	S-IPD	*S-POD & S-APOD*
$0.75 \leq m_a$	9	5
$0.5 < m_a < 0.75$	7	3
$0.25 < m_a < 0.5$	5	-

It is clear from Fig. 16, that the simulation and experimental results are close to each other.

From the THD point of view from figure (17) it is clear that the best technique is the S-IPD because it gives the lowest THD for the output voltage for all values of m_a. While the S-POD and S-APOD are almost the same.

From the output voltage point of view it is clear that from Fig. 18, the output voltage RMS value for the three techniques are similar and it increases linearly at $0 < m_a \leq 1$.

All the experimental setups in this paper have been conducted at the Electrical Engineering Department, Benghazi University. It was found that there is a good agreement between the simulation and the experimental results throughout the work of this study.

VII. CONCLUSION.

One of the important research points in multilevel inverters is the quality of the output voltage. The PWM control technique is used to improve the output voltage quality of the inverter; because the modulation technique which is used for control of switches of the multilevel inverter influences the harmonic contents of the output voltage. The goal of this paper is to study and compare three modulation techniques based on multicarrier level shifted PWM in order to know which technique gives the better output voltage quality. All methods are tested using MATLAB Simulink in addition to an experimental five-level inverter circuit, and the obtained results are coherent.

All obtained results revealed that among the methods under study, the *S-IPD* method results in a better output voltage quality than the other two techniques (*S-POD* and *S-APOD*) in terms of THD, Harmonic spectrum, number of levels and the *dv/dt* stress points of views. This is true for all values of amplitude modulation ratios.

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