Comparison of Different Third Harmonic Injected PWM Strategies for 5-Level Diode Clamped inverter

Mohamed Elrais Tamasas
Electrical and Electronic Dep.
University of Benghazi
Benghazi, Libya
mohamed.tamasas@uob.edu.ly

Mohammed Saleh
Electrical and Electronic Dep
University of Benghazi
Benghazi, Libya
bargathy81@yahoo.com

Mahmoud Shaker
Electrical and Electronic Dep
University of Babylon,
Hilla, Iraq
mahmoud111957@yahoo.com

Ahmed Hammoda
Electrical and Electronic Dep
University of Benghazi
Benghazi, Libya
ahmed.hammoda@uob.edu.ly

***Abstract*—In this paper, three modulation strategies based on a multicarrier level shifted PWM and third harmonic injected reference have been implemented; the aim of this paper is to compare these three strategies to know their effect on the output voltage quality of the inverter. The three modulation strategies are: Third Harmonic Injected reference In Phase Disposition (*THI-IPD*), Third Harmonic Injected reference Alternative Phase Opposition Disposition (*THI-APOD*) and Third Harmonic Injected reference Phase Opposition Disposition (*THI-POD*). These three strategies are applied to the single phase 2-legs 5-levels diode clamped inverter under different operation conditions. The study has been implemented via simulation using MATLAB/Simulink and setup experiments in the lab and the comparison between the simulation and experimental results are provided.**

***Keywords*—5-level DC inverter, Third Harmonic Injected reference, level shifted PWM, THI-IPD, THI -POD and THI -APOD.**

I. Introduction

Flying capacitor, Cascade and Diode clamped are the most popular multilevel inverter topologies. Numerous modulation strategies have already been reported to control the switches of these topologies. Of these modulation strategies, carrier-based modulations are considered the most common ones because of their inherent simplicity and their decreased computational requirements. Carrier-based modulation strategies are frequently established based on the carrier disposition technique for Diode-Clamped inverters, while they are extensively based on phase shifted technique for Cascade inverters. Each modulation strategy has its features which can be preferable or not preferable for a specific application [1]-[2].

II. Single Phase 2-legs 5-Levels DC Inverter

The topology that has been used in this paper is a single phase 2-legs five levels diode clamped inverter as shown in Fig. 1. With ***m*** being the number of output voltage level per leg (V_{An}, V_{Bn}), which is in this case equal to five. In general, the ***m*** level diode clamped inverter leg has ***(m-1)*** *dc* voltage inputs or *dc* link capacitor, ***2(m-1)*** switches per leg. The rating voltage of each switch is one *dc* voltage (V_{dc}) because when it is reversed it blocks a voltage level equals to V_{dc}. The required number of clamping diodes per leg *is* ***(m-1)*** × ***(m-2)*** if the inverter is designed such that each clamping diode has the same voltage rating as the switches and the minimum diode reverse voltage is equal to V_{dc}. Otherwise, *2(m-2)* clamping diodes are required per leg with different ratings for reverse voltage blocking [3].

The output voltage for the Single Phase 2-legs 5-levels Diode Clamped Inverter per leg for each switching configuration is shown in table I.

It is clear from *table I* that there are not redundant switching configurations per leg for any *m*-level diode-clamped inverter leg; also, at any time there are *(m-1)* consecutive switches in *On* states, conducting. As the series of conducting switches moving from the top to the bottom end of the leg, the output voltage decreases from $2V_{dc}$ to $-2V_{dc}$ when the output is taken from V_{An} [3]-[4].

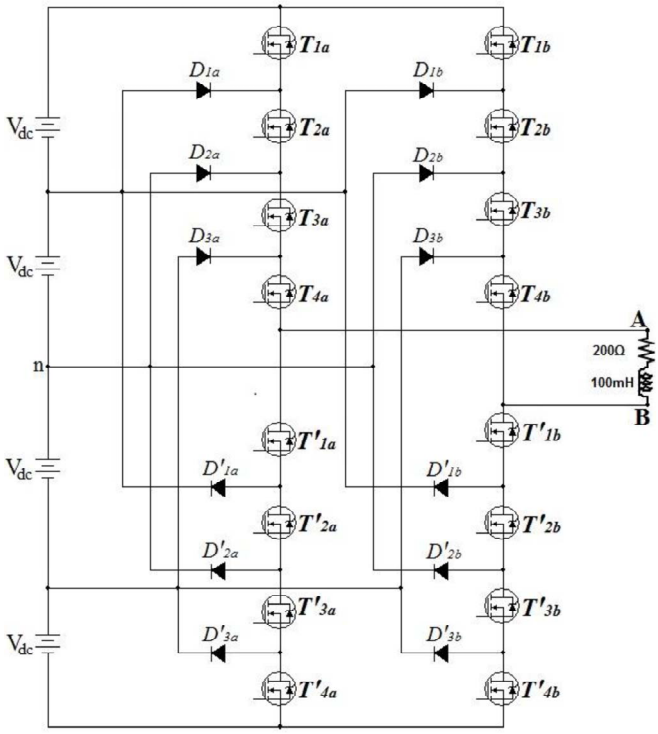


Fig. 1. Single phase 2-legs five levels diode clamped inverter.

TABLE I
THE OUTPUT VOLTAGE FOR EACH SWITCHING STATES

T_{1a}	T_{2a}	T_{3a}	T_{4a}	T'_{1a}	T'_{2a}	T'_{3a}	T'_{4a}	V_{An}
1	1	1	1	0	0	0	0	$2V_{dc}$
0	1	1	1	1	0	0	0	V_{dc}
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-V_{dc}$
0	0	0	0	1	1	1	1	$-2V_{dc}$

978-1-5090-5550-0/17/$31.00 ©2017 IEEE

III. MODULATION STRATEGIES

In this paper, three modulation strategies have been conducted based on multi carrier level shifted PWM using third harmonic injected reference signal that obtained by adding the third harmonic sinusoidal signal with 1/6 of the peak of the fundamental to the fundamental sinusoidal signal to increase the fundamental component to 15% [5], as shown in Fig. 2. The three strategies have the same operation principle as follow:

The numbers of the needed carriers are (*m-1)* for *m*-level multilevel inverter, all carriers have identical frequency f_c and peak-to-peak amplitude A_c. However, these carriers are shifted in levels to form adjacent bands. The numbers of the needed

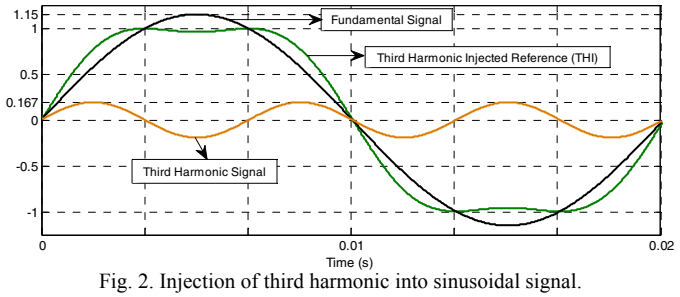


Fig. 2. Injection of third harmonic into sinusoidal signal.

reference signals have identical frequency f_r and peak-to-peak amplitude A_r, but they are out of phase. The two reference signals are positioned in the middle of the carriers bands. The two references are constantly compared with each of the carrier signals. If the reference is greater than the carrier, then the switch related to that carrier is switched *On*; and if the reference is less than the carrier, then the switch related to that carrier is switched *Off* as shown in Fig. 3.

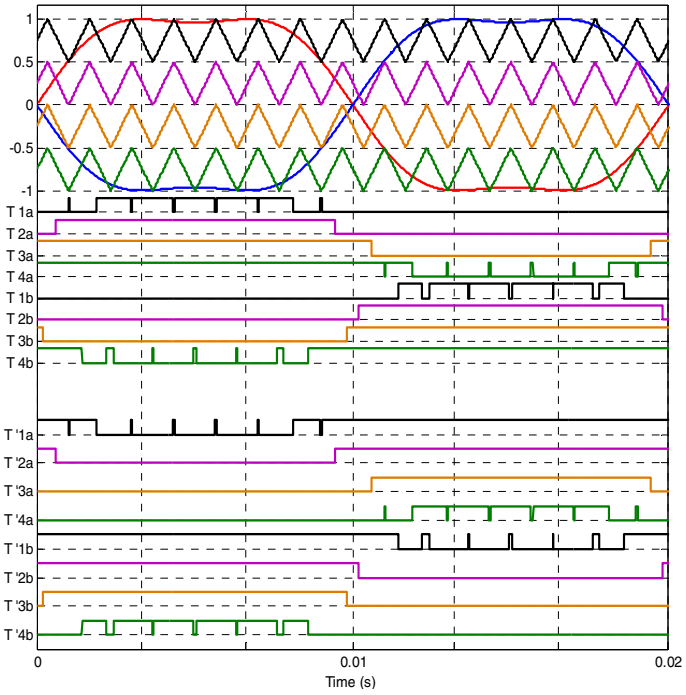


Fig. 3. Third harmonic injected reference PWM strategy with the train of pulses used to control the single phase 2-legs 5-level inverter, $m_a=1, m_f= 15$

The mathematical expression for the amplitude modulation ratio (m_a) and the frequency modulation ratio (m_f) are shown in (1) and (2) respectively [3], [6]-[7]. And the analytical expression for the reference signal is shown in (3) [5].

$$m_a=A_r/(m-1)*A_c \quad (1)$$

$$m_f=f_c/f_r \quad (2)$$

$$V_r(t)=1.15*m_a\,(Sin(w_1t)+ Sin(3w_1t)) \quad (3)$$

The three modulation strategies that have been compared in this paper are as follow:

A. *Third Harmonic Injected reference In Phase disposition technique (THI-IPD).*

In this method the carriers are the same in the frequency, amplitude and phases, they are just different in DC offset to occupy contiguous bands. The waveforms of the carriers of this strategy with third harmonic injected reference are illustrated in Fig. 4.

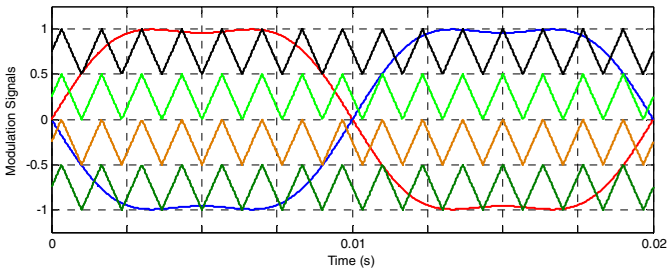


Fig. 4. The waveforms of the carriers with third harmonic injected reference for *THI-IPD* strategy, $m_a=1$,$m_f= 15$.

B. *Third Harmonic Injected reference Alternative Phase Opposition Disposition (THI-APOD).*

In this method the carriers are identical, but they are different in their DC offset and their phases are different where each carrier band is shifted by 180 degrees from the adjacent bands. The waveforms of the carriers of this strategy with third harmonic injected reference are illustrated in Fig. 5.

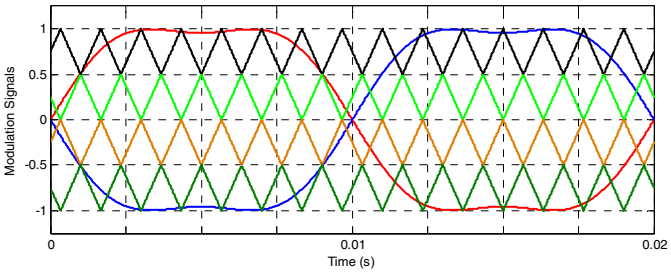


Fig. 5. The waveforms of the carriers with third harmonic injected reference for *THI- APOD* strategy, $m_a=1$, $m_f= 15$.

C. *Third Harmonic Injected reference Phase opposition disposition (THI-POD).*

Carriers in this method are the same in frequency and amplitude but they are different in phase and DC Offset where the carriers above the zero reference are in phase but shifted

by 180 degrees from those carriers below the zero reference. The waveforms of carriers of this strategy with third harmonic injected reference are illustrated in Fig. 6.

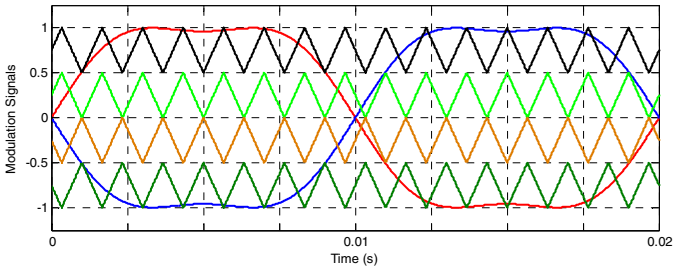


Fig. 6. The waveforms of the carriers with third harmonic injected reference for *THI- POD* strategy, m_a=*1*, m_f= *15*.

IV. Software And Hardware

A visual basic program has been used to generate the firing signals and they have been exported to the switches of the power inverter through the parallel port as shown in fig. 7.

After the generated signals exported through the computer's parallel port (8 lines for T_{1a} to T_{4a} and T_{1b} to T_{4b}), the following hardware components are added (refer to fig.7.):

1. Logic Inverters 4704 to obtain the signals for T'_{1a} to T'_{4a} and T'_{1b} to T'_{4b}.
2. Isolation circuit, the goal is to isolate the computer from the power circuit and to prevent short circuit occurrence between switches. For isolation the IC 4N25 (16 units) is used.
3. For the power switches of the main inverter the IRF530 MOSFETs (16 units) have been used.
4. The clamping diodes that have been used in the circuit are BY359-1500 diode (12 units).
5. Four DC supply each of V_{dc}=27V to construct the full DC-link voltage.
6. The AC-load that has been used is reactive load of 100mH inductor with rated current of $I_{L\text{-}rated}$=0.5A and 200Ω resistor.

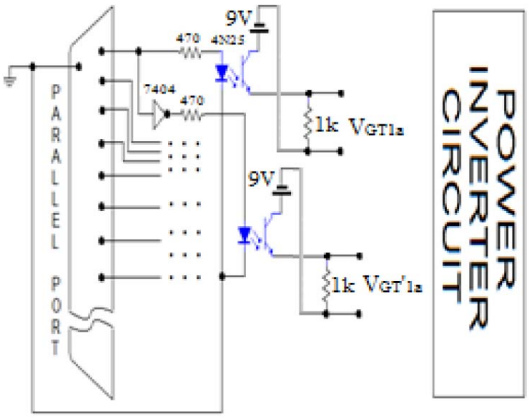


Fig. 7. Power circuit's block diagram.

A photo of the experimental single-phase 2-legs 5-level inverter considered in this paper is shown Fig. 8.

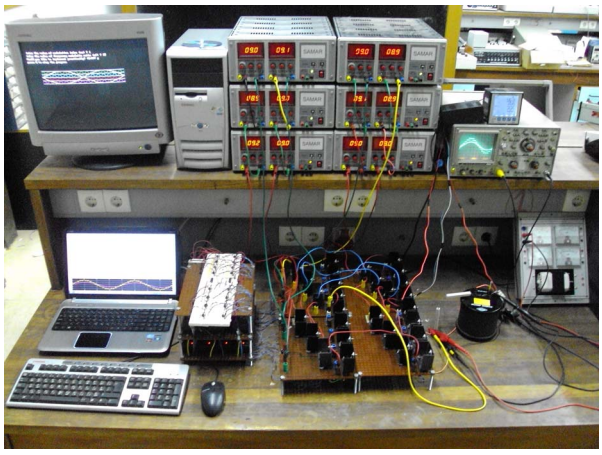


Fig. 8. A photo of the experimental single-phase 2-legs 5-level inverter.

V. Simulation And Experimental Results

The overall setup (the three modulation strategies compared in this paper with the inverter power circuit) was implemented via simulation using MATLAB/Simulink and experimentally in the lab and operated for different values of m_a. This paper presents samples of the obtained results to compare the three modulation strategies mainly from the *THD* and harmonic spectrum points of views for various values of m_a and m_f.

Despite the fact that the inverter is single phase 5-level, the output voltage waveform generated using the *THI-IPD* strategy at m_a=1 and m_f =18 is formed of 9-levels and each level has an amplitude equals to $1V_{dc}$ as shown in Fig.9 (a) and Fig. 10 (a).

The number of levels that form the output voltage generated using the other two strategies (*THI-POD and THI-APOD*) are 5-levels and each level has an amplitude equals to $2V_{dc}$ resulting in higher d_v/d_t stress on the components in comparison to *THI-IPD* as shown in Fig.11 (a) to Fig. 14 (a).

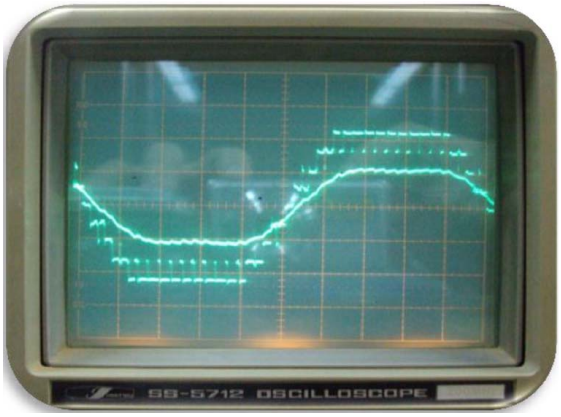
The number of levels generated by each modulation strategy depends on the value of the amplitude modulation ratio (m_a) as shown in table II.

The presence of the third harmonic component in the spectrum of the output voltage is because of the third harmonic component that was injected to the fundamental component to form the reference signal as shown in Fig. 9 (b) to Fig. 14 (b)

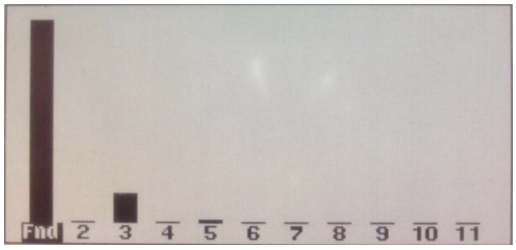
Table II

The Number Of Levels That Form The Output Voltage For Various Values Of M_A

Amplitude Modulation Ratio (m_a)	Number Of Output Voltage Levels	
	THI -IPD	*THI -POD & THI -APOD*
0.75≤ m_a	9	5
0.5<m_a<0.75	7	3
0.25<m_a<0.5	5	-

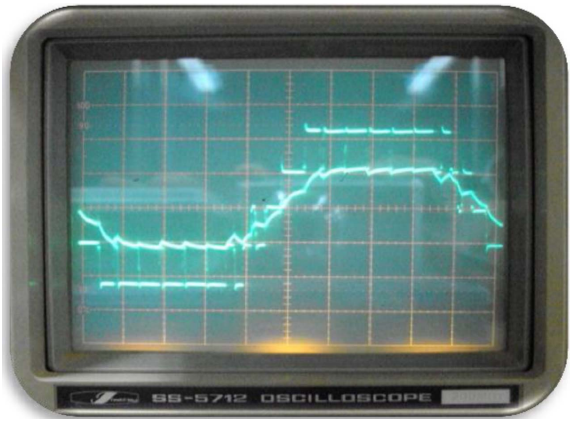


(a) ch1 (50v/Div), ch2 (0.4A/Div), 2ms/Div

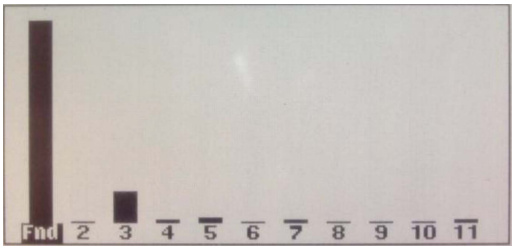


(b)

Fig. 9. *THI-IPD*, m_a=1, m_f =18, (a) Experimental output voltage and current, (b) Output voltage harmonic spectrum.

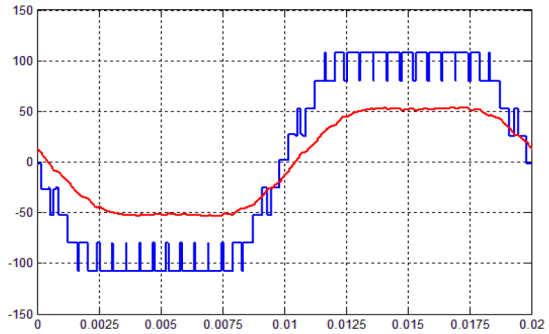


(a) ch1 (50v/Div), ch2 (0.4A/Div), 2ms/Div

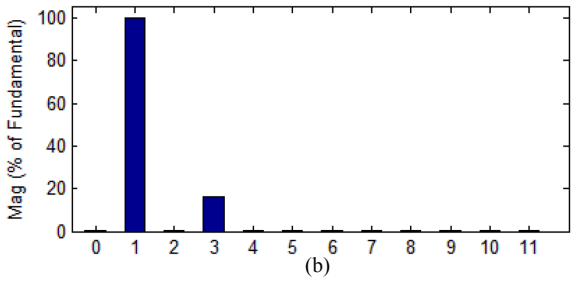


(b)

Fig. 11. *THI-POD*, m_a=1, m_f=18, (a) Experimental output voltage and current, (b) Experimental output voltage harmonic spectrum

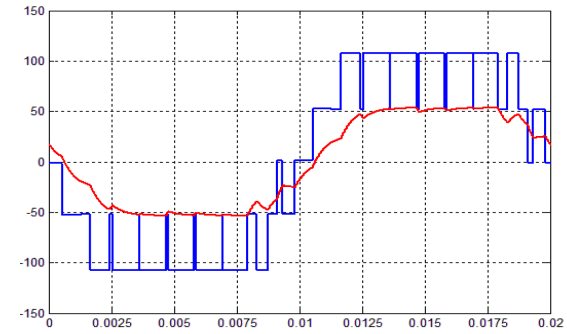


(a) Current enlarged with scale 100

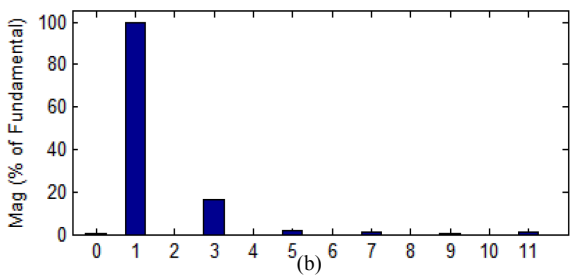


(b)

Fig. 10. *THI-IPD*, m_a=1, m_f =18, (a) Output voltage and current via simulation, (b) Output voltage harmonic spectrum via simulation

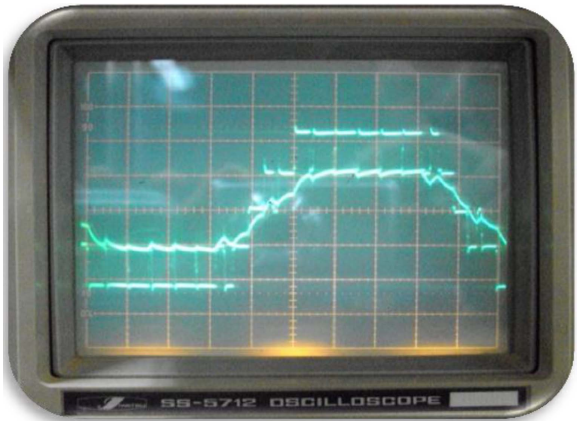


(a) Current enlarged with scale 100

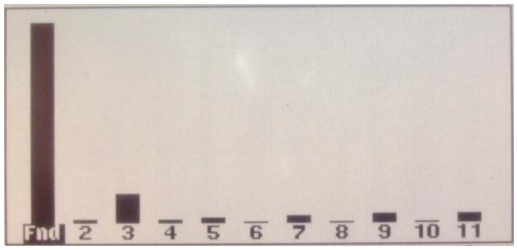


(b)

Fig. 12. *THI-POD*, m_a=1, m_f=18, (a) Output voltage and current via simulation, (b) Output voltage harmonic spectrum via simulation

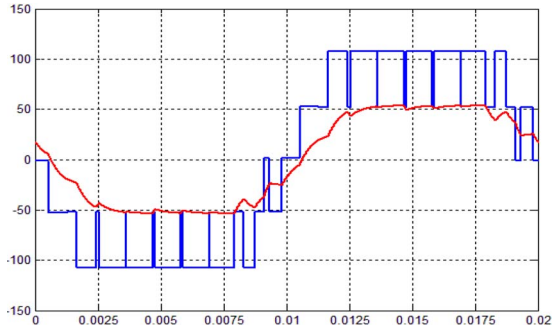


(a)ch1(50v/Div), ch2(0.4A/Div), 2ms/Div

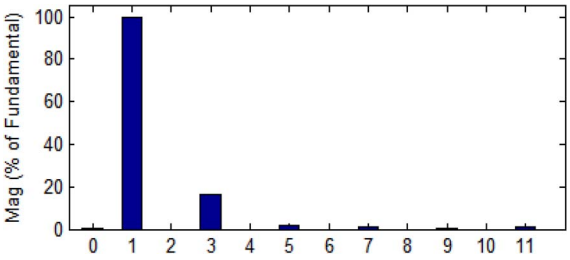


(b)

Fig. 13. *THI-APOD*, m_a=1, m_f=18, (a) Experimental output voltage and current, (b) Experimental output voltage harmonic spectrum



(a) Current enlarged with scale 100



(b)

Fig. 14. *THI-APOD*, m_a=1, m_f=18, (a) Output voltage and current via simulation, (b) Output voltage harmonic spectrum via simulation.

The simulation results matches with the experimental results as shown in Fig. 15. The modulation strategy that produces more output voltage levels is better because it produces lower *THD*; The *THI-IPD* strategy is the best among the other two strategies, *THI-POD* and *THI-APOD*, because it has the lowest *THD* for all value of m_a and *THI-POD* and *THI-APOD* are identical as shown in Fig. 16.

The RMS value of the output voltage for all strategies are the same and increase linearly at $0<m_a\leq 1$ as shown in Fig. 17.

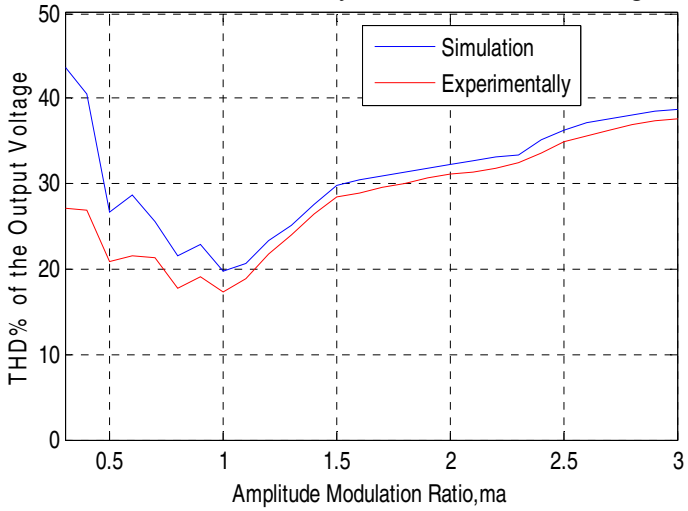


Fig. 15. *THD vs* m_a of the output voltage at m_f=18 for *THI-IPD* strategy via simulation and experimentally.

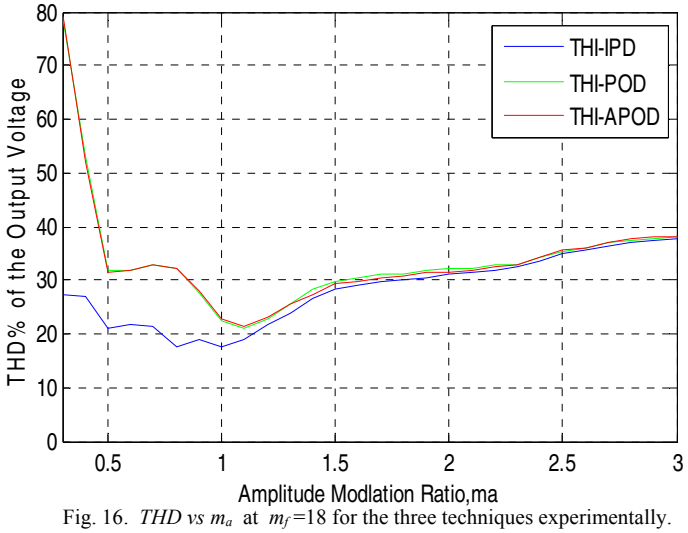


Fig. 16. *THD vs* m_a at m_f=18 for the three techniques experimentally.

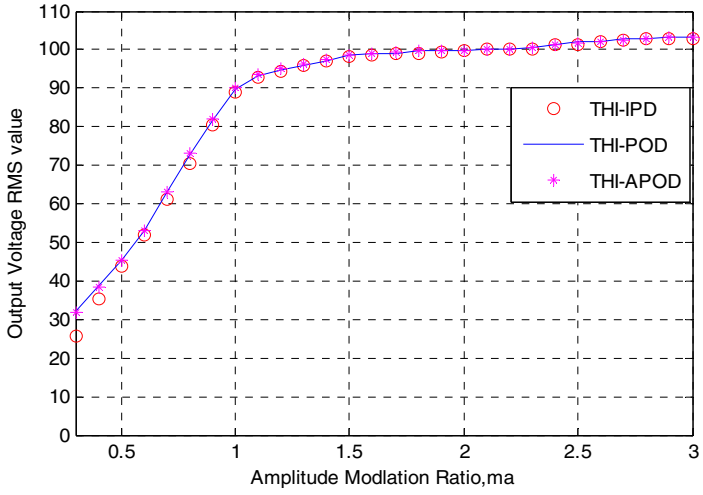


Fig. 17. V_{rms} vs m_a at m_f=18 for the three strategies experimentally.

VI. CONCLUSION

The *THI-IPD* strategy is the best from the *THD*, Harmonic spectrum, number of output voltage levels and the dv/dt stress points of views and this is true for all values of m_a.

The *THI-POD* and *THI-APOD* strategies are almost the same for all values of m_a.

The *RMS* output voltage for all the three strategies are the same for all values of m_a.

The dispositioning strategies that use third harmonic injected reference provide better DC voltage usage, in other words, it produces higher output voltage than the ones that use the pure sinusoidal reference at the same value of m_a as compared with [8].

The output voltage produced using using third harmonic Injected reference is higher than the output voltage produced in [8] using pure sinusoidal reference by almost 15% because the third harmonic component that was injected to the fundamental component is one-sixth of the fundamental and this is the maximum percent increase as proved in [5].

One disadvantage in using the third harmonic injected reference in the single phase multilevel inverter is the presence of the third harmonic component in the output voltage.

REFERENCES

[1] S. Jeevananthan, R. Madhavan, T. Suresh Padmanabhan and P. Dananjayan,"State-of-the-art of multi-carrier modulation techniques for seven level inverter: A critical evaluation and novel submissions based on control degree of freedom," *Industrial Technology, 2006. ICIT 2006 IEEE International Conference* , 2006, pp. 1269-1274.

[2] S. S. Fazel, "Investigation and Comparison of Multi-Level Converters for Medium Voltage Applications," Ph.D. dissertation, Technical Univ of Berlin., Berlin., 2007.

[3] A. Lega. "Multilevel Converters: Dual Two-Level Inverter Scheme," Ph.D. dissertation, Dept. Elect. Eng., Univ of Bologna., Bologna, Italy, 2007.

[4] Y. Liu, "Advanced Modulation, Control and Application for Multilevel Inverters, " Ph.D. dissertation, North Carolina State Univ, Raleigh, North Carolina, 2009.

[5] J. A. Houldsworth and D. A. Grant, "The use of harmonic distortion to increase the output voltage of a three-phase PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-20, pp. 1224-1228, Sept. 1984.

[6] S. Khomfoi and L. M. Tolbert, "Multilevel Power Converters", in M. H. Rashid, *Power Electronics Handbook - Devices, Circuits, and Applications*, 3rd ed. Elsevier, 2011, ch.17,pp. 455-484.

[7] Z. Daneshi Far, A. Radan and M. Davari Far, "Introduction and evaluation of novel multi-level carrier-based pwm strategies using a generalized algorithm", *Power Electronics and Applications 2007 European Conference*, 2007, pp. 1-10.

[8] M. Tamasas, M. Saleh, M. Shaker, A. Hammoda, "Evaluation of modulation techniques for 5-level inverter based on multicarrier level shift PWM", *Proc. IEEE Mediterranean Electrotech. Conf.*, pp. 17-23, Apr. 2014.